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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,712	09/30/2003	Ken Drottar	884.A81US1	2957

21186 7590 09/18/2007

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EXAMINER	
WHITE, DYLAN C	

ART UNIT	PAPER NUMBER
2819	

MAIL DATE	DELIVERY MODE
09/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/676,712	DROTTAR ET AL.	
	Examiner	Art Unit	
	Dylan White	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 12-23* is/are rejected.

7)☒ Claim(s) *11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 July 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claim 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments filed 6/21/2007 with regards to the prior art Reference of Arcoleo et al (U.S. Pat. 5,864,506) have been fully considered but they are not persuasive.

Regarding Applicants arguments of claim 1, the Examiner disagrees with the application regarding the disclosure of suggestion of claim 1. The Examiner explained in the previous office action and directly pointed out two transistors that formed a first inverter connected at the source/drain to each other, where the second transistor was larger than the first.

Additionally the Examiner respectfully disagrees with the Applicants interpretation of transistor sizing discussed in Arcoleo. Applicant asserts that there is no description of any transistors having a size that is different from any other of the transistors and that according to the description the transistors have the same length, width, capacitance, or channel resistance could be selected to provide drive strength magnitude. Nowhere does Arcoleo disclosed that all transistors are of the same size, and it is disclosed that the drive strength of each and every transistors is open to be changed based on the transistors characteristics and desired circuit design. Additionally as the Applicant

stated the same length, width, capacitance, and channel resistance "could be" selected to provide a drive strength. It could be selected that way but it is clear that not all transistors have to have the same characteristics.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., no mention of compensation for slow response) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Additionally in response to applicant's argument that the Office Action does not address or make mention of compensation for a slow response, the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

The Applicant also argues that Arcoleo does not disclose or suggest different sizes for the transistors based on the different types. The Examiner disagrees because it is very well known in the art that the different types of transistors (PMOS, NMOS) have sizes that are different from each other. Additionally since Arcoleo states that transistors 501a, 501b, 502a, and 502b each have physical characteristics length,

width, capacitance, and channel resistance; each of the four transistors can differ from each other.

In response to Applicants argument regarding MPEP 2144.04 IV; A change is size is generally recognized as being within the level of ordinary skill in the art. Changing the physical size of the transistor does not change the functionality of the transistor or the inverter circuit (it may change the threshold voltage of the transistor but it does not change the function of the transistor (switching on/off) or the function of the inverter (switching high to low)) in which the transistor resides and therefore is generally regarded as within the level of ordinary skill in the art. Therefore the case law as stated in 2144.04 IV does properly apply to the subject matter of claim 1. Additionally it is extremely well know in the art that changing the size of a transistor will effect the speed at which a transistor switches; larger transistors switch slower while smaller transistors switch faster and it is also well know in the art that equal size PMOS and NMOS transistors do not switch at the same speeds.

The Examiner had previously provided explanation and motivation for the combination of Arcoleo in view of Marshall for claims 1-20 and therefore met the burden of establishing a *prima facie* case of obviousness.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the second transistor larger than the first transistor must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Additionally there is no support in the drawings to show where the first circuit is size with respect to the second circuit.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-10 and 12-15, are rejected under 35 U.S.C. 103(a) as being unpatentable over Urakami et al. (U.S. Pat. 6,794,909) in view of Arcoleo et al. (U.S. Pat. 5,864,506).

Regarding claim 1, Urakami discloses a first circuit (transistors 19 & 20 @ Fig. 2) couple to an input port (input) of the transmitter (Fig. 2), the first circuit including an input port (gates of transistors 19 & 20) and an output port (at node N11) and no more than two transistors (19 & 20) including a first transistor (19) having a source/drain directly connected to a source/drain of the second transistor (20), and a second circuit (transistors 21, 22, 27.1-n, and 28.1-n) including a second circuit input port (gates of transistors 21 & 22) to the output port of the first circuit (node N11), the second circuit including an output port (node N12) coupled to the output port of the transmitter (output), where the first circuit (transistors 19 & 20) is sized with respect to the second circuit (transistors 21, 22, 27.1-n, and 28.1-n) such that for a pulse applied to the input port of the transmitter, the transmitter generates an output signal having a rise-time and fall-time substantially equal (turning on and off transistors 27.1-n and 28.1-n will size the second circuit to produce an output signal having rise and fall times substantially equal at the output port).

Urakami fails to disclose where the second transistor (20) is larger than the first transistor (19).

Arcoleo discloses an output driver where the size of a transistor (501b) in an inverter (transistors 501a & 501b) can be selected based on the physical characteristics (col. 8, lines 20-26), where the N-type transistor can be larger that the P-type transistor. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use the output drive (transmitter) circuit as disclosed by Urakami with the transistor sizing as taught by Arcoleo for impedance matching and improved signal quality.

Regarding claim 2, the combination discloses where the first circuit includes an inverter (Urakami; transistors 19 & 20 @ Fig. 2).

Regarding claim 3, the combination discloses where the inverter includes n-type MOSFET (Urakami, 20 @ Fig. 2) in series with a p-type MOSFET (19).

Regarding claim 4, the combination discloses where the n-type MOSFET (Urakami; 20 @ Fig. 2) is larger than the P-type MOSFET (Arcoleo; col.8, lines 20-26).

Regarding claim 5, the combination discloses the claimed invention except for the n-type MOSFET being about two to three times larger than the p-type MOSFET. It would have been an obvious matter of design choice to make the n-type MOSFET

about two to three times larger than the p-type MOSFET, since such a modification would have involved a mere change in the size of a component (changing the size of a transistors does not change the function the function of the transistor (switching on/off) nor does it change the function of the inverter (switching high/low)). A change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose*, 105 USPQ 237.

Regarding claim 6, the combination discloses where the second circuit includes a plurality of driver circuits (Urakami, 27.1-n & 28.1-n @ Fig. 2).

Regarding claim 7, the combination discloses where each of the plurality of driver circuits (Urakami, Fig. 2) includes a p-type MOSFET (19, 21, 27.1-n) connected in series with an N-type MOSFET (20, 22, 28.1-n, respectively).

Regarding claim 8, the combination discloses where the P-type MOSFET (Urakami; 19 @ Fig. 2) is sized to source a first current (from VDD) and the N-type MOSFET is sized so sink a second current (to GND) substantially equal to the first current (the transistors have to be sized in order to handle substantially equal first and second currents, if the transistors were too small they would burn out).

Regarding claim 9, the combination discloses where the second circuit (Urakami, 21, 22, 27.1-n, and 28.1-n) is connected to an equalization control circuit (transistor controls for 27.1-n and 28.1-n).

Regarding claim 10, the combination discloses where the equalization control provides de-emphases (Urakami; col. 5, lines 19-26).

Regarding claim 12, Urakami discloses receiving a signal (at input @ Fig. 2) at a first circuit (transistors 19 & 20), the first circuit including an input port (input) and an output port (at node N11) and no more than two transistors (19 & 20) including a first transistor (19) having a source/drain directly connected to a source/drain of the second transistor (20); a second circuit (transistors 21, 22, 27.1-n, and 28.1-n) coupled to the first circuit (at node N11), the second circuit including a plurality of P-type MOSFET's (21, 27.1-n), enabling the plurality of P-type MOSFET's to drive a transmission line (connected to output); and enabling less than the plurality of P-type MOSFET's (via control signals 15.1-n) to drive the transmission line (not shown, connected to output). Where the first circuit (transistors 19 & 20) is sized with respect to the second circuit (transistors 21, 22, 27.1-n, and 28.1-n) such that for a pulse applied to the input port of the transmitter, the transmitter generates an output signal having a rise-time and fall-time substantially equal (turning on and off transistors 27.1-n and 28.1-n will size the second circuit to produce an output signal having rise and fall times substantially equal at the output port).

Urakami fails to disclose where the second transistor (20) is larger than the first transistor (19).

Arcoleo discloses an output driver where the size of a transistor (501b) in an inverter (transistors 501a & 501b) can be selected based on the physical characteristics (col. 8, lines 20-26), where the N-type transistor can be larger that the P-type transistor. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use the output drive (transmitter) circuit as disclosed by Urakami with the transistor sizing as taught by Arcoleo for impedance matching and improved signal quality.

Regarding claim 13, the combination discloses receiving a signal at a first circuit (transistors 19 & 20) includes receiving a digital signal (at input node).

Regarding claim 14, the combination discloses enabling the plurality of P-type MOSFET's (27.1-n) to drive a transmission line (at output node) includes enabling the plurality of P-type MOSFET's substantially simultaneously (enabling gate control signals).

Regarding claim 15, the combination discloses where enabling less than all of the P-type MOSFET's (27.1-n) to drive the transmission line (not shown, connected to output) comprises enabling less than all of the p-type MOSFET's substantially simultaneously (don't have to enable all PMOS transistors).

Claims 16-19, are rejected under 35 U.S.C. 103(a) as being unpatentable over Urakami et al. (U.S. Pat. 6,794,909) in view of Arcoleo et al. (US Pat. 5,864,506) in further view of Marshall et al. (U.S. Pat. 6,876,224).

Regarding claim 16, Urakami discloses a transmitter (Fig. 2) including a first circuit (transistors 19 & 20) coupled to an input port (input) of the transmitter, the first circuit including an input port (gates of transistors 19 &20) and an output port (node N11) and no more than two transistors (19 & 20) including a first transistor (19) and a second transistor (20), the first transistor having a source/drain directly coupled to a source/drain of the second transistor (Fig. 2) and a second circuit (transistors 21, 22, 27.1-n & 28.1-n) coupled to the first circuit (at node N11) to an output port of the transmitter (output), the second circuit coupled to an equalization control circuit (Fig. 2), where the equalization control provides de-emphasis (turns transistors 27.1-n & 28.1-n on/off);

Urakami fails to directly disclose the second transistor larger than the first transistor.

Arcoleo discloses where transistors can be sized with respect to each other based on the transistor length, width, capacitance, and channel resistance (col. 8, lines 20-26), therefore, It would have been obvious to one of ordinary skill in the art at the time of invention to use the transmitter disclosed by Urakami with the transistor sizing as taught by Arcoleo for adjusting the drive strength of each of the transistors.

The combination fails to disclose a receiver and a transmission line connecting the transmitter to the receiver. However, it is obvious that a receiver is required to receive the transmitted data, and that a transmission line would connect the two.

Marshall discloses a system (Marshall, Fig. 6) comprising components (602-610) where a transmitter and receiver are needed to communicate between the components of the system, and where bus lines (602) would constitute a group of transmission lines. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use the transmitter disclosed by the combination of Urakami and Arcoleo within the system taught by Marshall for impedance matching and improved signal quality.

Regarding claim 17, the combination discloses where the first circuit is an inverter (Urakami, 19 & 20 @ Fig. 2) having a P-type MOSFET (19) and an N-type MOSFET (20), the N-type MOSFET being between about two and about three times larger than the P-type MOSFET (Arcoleo; col. 8, lines 20-26). Furthermore (MPEP 2144.04 IV. A) it would have been an obvious matter of design choice to change the size of the N-type MOSFET, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose*, 105 USPQ 237.

Regarding claim 18, the combination discloses where the second circuit (Urakami; transistors 21, 22, 27.1-n & 28.1-n @ Fig. 2) includes a voltage driver (transistors 21 & 22).

Regarding claim 19, the combination discloses where the second circuit includes a controllable source impedance (Urakami; 27.1-n & 28.1-n @ Fig. 2).

Claim 20, are rejected under 35 U.S.C. 103(a) as being unpatentable over Urakami et al. (U.S. Pat. 6,794,909) in view of Marshall et al. (U.S. Pat. 6,876,224).

Regarding claim 20, Urakami discloses a first circuit (transistors 19 & 20) coupled to an input port (input) of the transmitter (Fig. 2); a second circuit (transistors 21, 22, 27.1-n, and 28.1-n) including a second input port (coupled to node N11) coupled to an output port of the first circuit (node N11), the second circuit including a second circuit output port coupled (N12) to the output port of the transmitter (output), where the first (transistors 19 & 20) and second (transistors 21, 22, 27.1-n, and 28.1-n) circuits are sized such that for an input signal the transmitter generates and output signal with a rise and fall time substantially equal to the input signal (turning on and off transistors 27.1-n and 28.1-n will size the second circuit to produce an output signal having rise and fall times substantially equal at the output port).

Urakami fails to disclose where a first and second processor transmit and receive signals respectively.

Marshall discloses drivers embodied in a system (col. 5, lines 54-55) with a first processor (Marshall; 604 left) and a second processor (604 right) where the transmitter (Urakami, Fig. 2) can transmit to a receiver (not shown, but obvious) through transmission line (Marshall; 602 @ Fig. 6), therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use the transmitter disclosed by Urakami with the system taught by Marshall for impedance matching to a transmission line for improved signal quality.

Claims 21-23, are rejected under 35 U.S.C. 103(a) as being unpatentable over Urakami et al. (U.S. Pat. 6,794,909) in view of Marshall et al. (US Pat. 6,876,224) in further view of Song (US Pat. 6,614,258).

Regarding claim 21, the combination of Urakami and Marshall disclose that of claim 20, but fail to disclose a specific type of processor.

Song discloses where a processor in a dynamic logic array can be a very long instruction word processor (VLIW, col. 9, line17), therefore, It would have been obvious to one of ordinary skill in the art at the time of invention to use the transmitter combination of Urakami and Marshall with the VLIW processor taught by Song for faster processing of more complex functions.

Regarding claim 22, where the second processor is a complex instruction set processor (CISC; Song, col. 9, line 16).

Regarding claim 23, the combination discloses an equalization control (Urakami, from nodes N15.1-n and N16.1-n @ Fig. 2) coupled to the second circuit (27.1-n & 28.1-n) to provide de-emphasis.

Allowable Subject Matter

Claim 11 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 11, where the transmitter transmits at a signal level and the first circuit and the second circuit are coupled to a supply potential having a value of at least twice the signal level.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dylan White whose telephone number is (571) 272-1406. The examiner can normally be reached on m-f 7:30- 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DW

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09/12/07